Connecting the DECchip 21140 PCI Fast Ethernet LAN Controller to the Network: An Application Note

Order Number: EC–QAR2A–TE

This document describes how to implement system and network connections to the DECchip 21140 PCI Fast Ethernet LAN Controller.

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1 Overview

This application note provides a basic description of how to implement 100BASE-TX and 10BASE-T network connections to the DECchip 21140 PCI Fast Ethernet LAN Controller (21140). The objective of this document is to help you successfully implement the 100BASE-TX and 10BASE-T network interface using the 21140.

Hardware design and layout recommendations are provided for hardware implementations that use the 21140. The software interface to the 21140 is not described here. For more information about 21140 software, refer to the Ordering Associated Literature section at the end of this document.

2 Functional Overview

This section describes both the host system interface and the network 100-Mb/s and 10-Mb/s interfaces. The host system interface is the peripheral component interconnect (PCI) bus.

2.1 System Interface

The 21140 has a single, 50-pin host system connection containing the PCI bus control and address/data signals.

The 21140 implements a direct interface to the PCI bus and has enough FIFOs for storage; therefore, it needs no external onboard memory. The 21140 uses DMA transfers to send and get packets to and from host system memory, minimizing host system workload.

The 21140 performs 33-MHz, synchronous DMA cycles when interfacing to the PCI board. This enables the board to operate on the PCI bus and utilize only 10 percent of the bus bandwidth during fully networked operation of 100-Mb/s Fast Ethernet reception or transmission. The bus master design provides for the highest possible throughput between the system and the network, yet it requires only a minimum of parts for a complete implementation.

2.2 Network Interface

The 21140 implements the 100BASE-TX media independent interface (MII) sublayer, the 100BASE-TX physical coding sublayer (PCS), and the 10-Mb/s and 100-Mb/s Ethernet media access control (MAC) sublayers. It provides a dual-network interface for both a 100BASE-TX and a 10-Mb/s Ethernet. The media independent interface/symbol (MII/SYM) port supports the industry-standard MII interface for any 100BASE-T or 100BASE-X implementation. It also provides additional functions for the 100BASE-TX interface, thus providing for a complete, highly integrated, low-cost 100BASE-TX solution. The 10-Mb/s port provides a standard, 7-wire interface between 21140 Ethernet MAC and front-end decoder (ENDEC) devices.

The 21140 supports two different modes to implement connection to its MII/SYM network port.

The first mode is the media independent interface (MII) mode. While in MII mode, the 21140 is fully compliant with the MII specifications as defined by the Fast Ethernet Alliance (FEA). The MII mode supports a nibble-wide, general interface that can be used with various physical interfaces, such as 100BASE-TX, 100BASE-T4, shielded twisted-pair (STP), and fiber cables. It also supports dual speed at the rates of 10 Mb/s and 100 Mb/s.

The second mode is the specific 100BASE-TX support mode. For this mode, the 21140 incorporates the PCS and the scrambling/descrambling function as specified in IEEE standard 802.3. While in this mode, the 21140 provides enhanced functionality for implementing a high-integration, low-cost 100BASE-TX connection using only a few additional standard twisted-pair physical layer medium dependent (TP-PMD) parts.

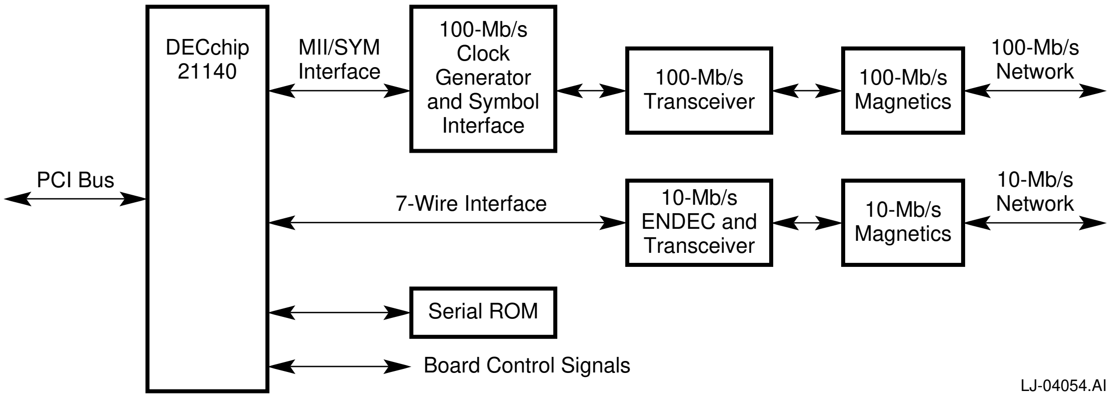
This document provides all the information you need to implement 100BASE-TX and 10-Mb/s network connections to the 21140. This document does not describe MII mode usage and operation.

This document describes a network connection solution that uses the DECchip 21140 PCI Fast Ethernet Evaluation Board (EB140). For more information about the evaluation board, refer to the *DECchip 21140 PCI Fast Ethernet Evaluation Board User Guide*.

3 Network Connections

Figure 1 shows a block diagram of the physical layer design for 100BASE-TX and 10BASE-T connections.

Figure 1 Network Interface



The following components are used to build this interface:

- 21140

  The 21140 incorporates the PCI system bus interface, the DMA engine, the FIFO buffers, the media access control (MAC), the physical coding sublayer (PCS), and the scrambler/descrambler.

- 100-Mb/s Clock Generator and Symbol Interface

  The clock recovery and symbol interface converts the 125-MHz NRZI encoded bit stream to 5-bit symbols at a rate of 25 MHz and converts 5-bit symbols at a 25-MHz rate into an NRZI encoded bit stream at 125 MHz. The Motorola MC68836 is used for this function in this application note.

- 100-Mb/s Transceiver

  The transceiver converts the NRZI bit stream to the MLT-3, three-level coding scheme and converts the MLT-3, three-level coding scheme to the NRZI bit stream. It also provides equalization to overcome received signal-level degradation with various cable lengths. The Micro Linear part number ML6671 is used for this function in this application note.

- 100-Mb/s Magnetics

  The 100-Mb/s magnetics contains isolation transformers and common mode choke transformers. Pulse Engineering part number PE68509 is used for this function in this application note.

- 10-Mb/s ENDEC and Transceiver

  The 10-Mb/s ENDEC and transceiver is the interface between the standard, 7-wire interface of the 21140 and the network connection, including all clock generation and recovery. The Level One part number LXT901 is used for this function in this application note.

- 10-Mb/s Magnetics

  The 10-Mb/s magnetics contains the transformers and serial chokes that the LXT901 requires for normal operation with 10BASE-T network connection. The Valor part number ST7010 or Fil-Mag part number 23Z356SM is used for this function in this application note.

3.1 100BASE-TX Network Implementation

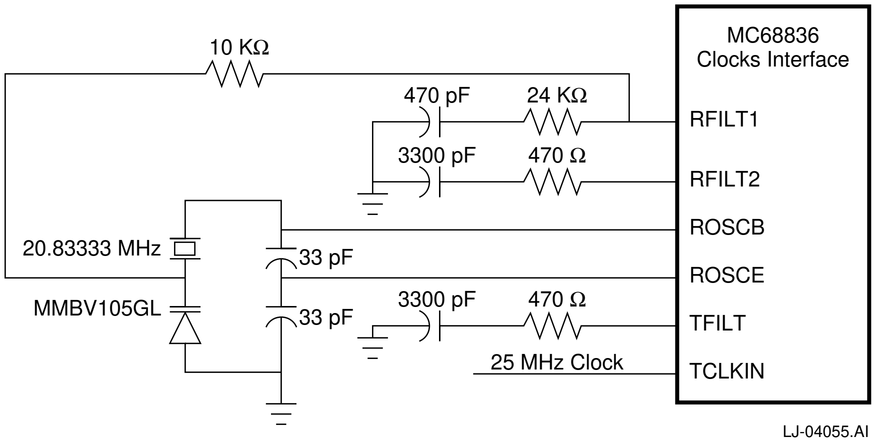
The 100BASE-TX network implementation is described in this section.

3.1.1 100-Mb/s Clock Generator and MII/SYM Port Interface—MC68836

The MC68836 is connected to the 21140 symbol interface, including the TX, RX, and clock signal lines. The MC68836 has a full symbol interface compatible with the 21140, and it also has a mechanism to recover the RX clock from the incoming network data bit stream (25-MHz clock). The MC68836 has a pseudo ECL interface port (125-MHz NRZI lines) to the MLT-3 transceiver, including the TX, RX, and SD lines.

3.1.1.1 Clocks Figure 2 shows the MC68836 phase-locked loop (PLL) receive clock recovery signal connections and the transmit clock connections and filters.

Figure 2 MC68836 Receive and Transmit Clock Connections



The receive PLL circuit includes a Motorola Varactor Diode (MMBV105GL) and a 20.833333-MHz receive crystal. Table 1 contains the required receive crystal specifications.

Table 1 Receive Crystal Specifications

Parameter	Value	Unit
Frequency	20.833333	MHz
Load capacitance	7.8 ±0.2	pF
Frequency tolerance	±10	PPM
Agian	±5	PPM/yr
Temperature stability (0°C–70°C)	±15	PPM
Oscillation mode	Fundamental	–
Parameters at 25°C ±2°C, Drive Level = 0.5 mW		
Shunt capacitance	7±1	pF
Motional capacitance	±5	fF
Co/Cm ratio (maximum)	245	–
Series resistance	20	Ω
Spurious responses	>5 dB below main within 500 KHz	–

The Standard Crystal part number 800T-20.83333-8 is recommended.

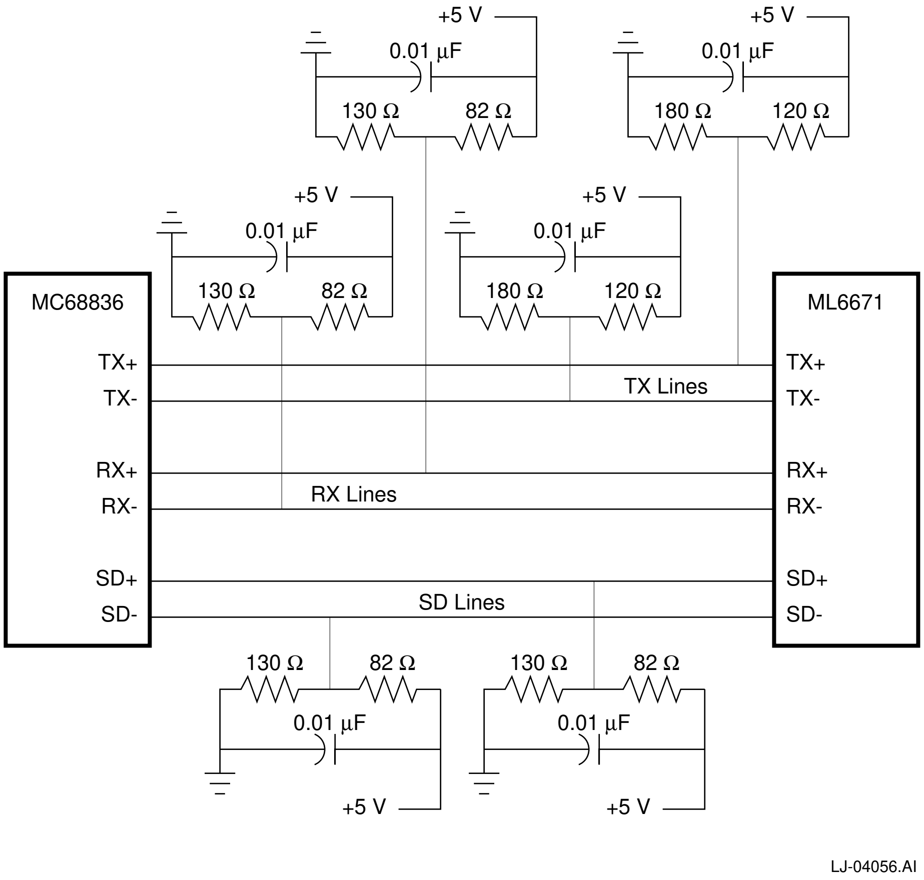
An external crystal oscillator is used for transmit clocking. It is the same part as the 25-MHz clock oscillator that drives the 21140 MII clock. Table 2 lists the required transmit crystal clock specifications.

Table 2 Transmit Crystal Clock Specifications

Parameter	Value	Unit
Frequency	25.0	MHz
Frequency tolerance	±50	PPM
Temperature stability (0°C–70°C)	±50	PPM

3.1.1.2 MC68836 Transceiver Interface The MC68836 transceiver is connected to the MLT-3 transceiver by pseudo ECL lines as shown in Figure 3. The three pseudo ECL pairs, SD ±, RD±, and TD±, should be terminated for impedance matching and for setting the dc bias level of the lines. Various terminations can be used.

Figure 3 Termination Network for MC68836—MII/SYM Port Interface



The termination arrangement shown in Figure 3 is used mostly for short lines and is implemented on the 21140 evaluation board. This termination circuit should be located as close as possible to the receiving side. For SD and RD pairs it should be close to MC68836 (FCG), and for the TD pair it should be close to the transceiver pins (ML6671 TXIN pair).

A filter capacitor on the signal lines is also recommended. For the termination nets layout consideration, refer to Section 8.2.3.

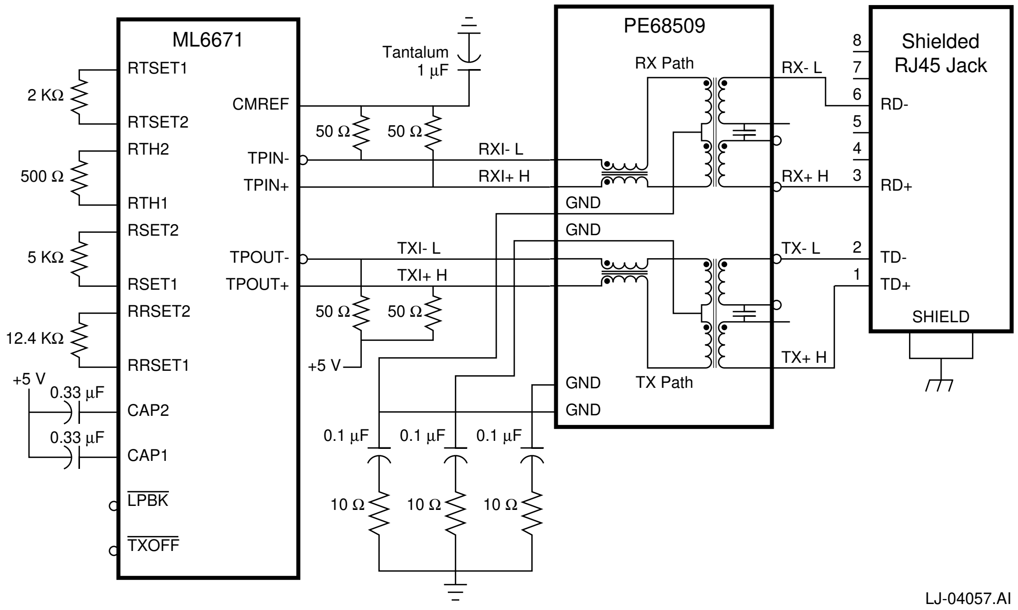
3.1.1.3 Loopback This function is optional and is not required for normal operation of the 100BASE-TX interface. When MC68836 input $\overline{LB}$ is asserted (low) the MC68836 disconnects the receive network input lines and loops the transmit data into the receive path. The NRZI (pseudo ECL) transmit lines are forced to the quiet state during loopback. The 21140 provides a very easy and straight forward way to support such a function, using one of the general-purpose pins (**gep<7:0>**). In order to do so, and to have this function be software controlled, the driver software should include such specific support. For more information, refer to the *DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual*.

3.1.2 ML6671 Transceiver (MLT-3)

The ML6671 transceiver is the interface between the 100-Mb/s clock generator and symbol interface chip, MC68836, and the network magnetics. The ML6671 has a pseudo ECL interface, which operates at a rate of 125 MHz, connected to the MC68836. The ML6671 has an MLT-3 interface that connects directly to the network magnetics.

3.1.2.1 ML6671 Network Connections Figure 4 shows all ML6671 network connections and required external parts. Refer to Section 3.1.1.2 for information about the MC68836 connection.

Figure 4 ML6671 Network Connection and External Components



3.1.2.2 Loopback The $\overline{LPBK}$ input is used for transceiver-level loopback. When loopback is asserted, the transceiver does not transmit on TPOUT ± and it loops back the TXI± input signals through the MLT-3 transceiver to the RXI ± pair of pseudo ECL lines.

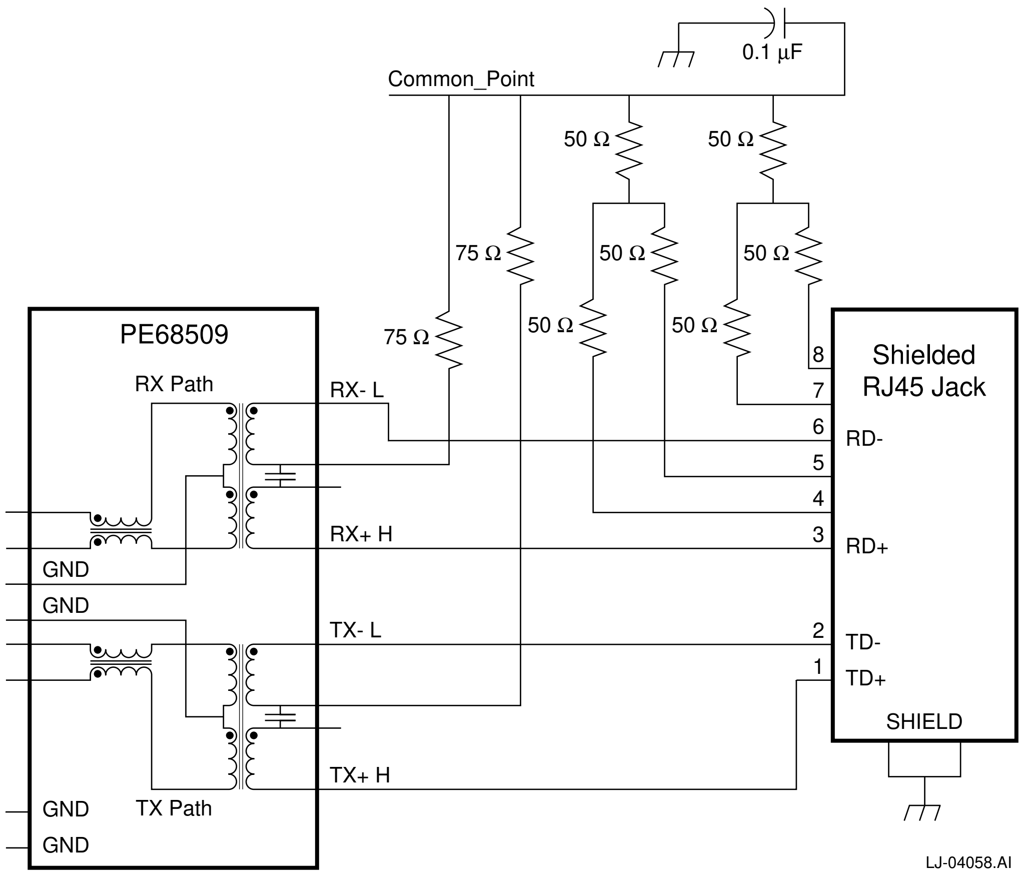
This function can be used for testing operation of the interface, as it covers most of the participating components in the 100BASE-TX implementation. The 21140 provides a very simple and convenient way to support loopback testing through one of its general-purpose pins (**gep<7:0>**). Note that to do this and to have this function be software controlled, the driver software should include such specific support. For more information, refer to the *DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual*.

3.1.3 PE68509 Magnetics

The Pulse Engineering part number PE68509 is a standard magnetics for 100BASE-TX implementation. It includes the transformers and serial chokes.

The module connections to the MLT-3 transceiver are shown in Figure 4. Figure 5 shows the magnetics interface to the RJ45 connector. The 100-Mb/s RJ45 unused pins (4, 5, 7, 8), connected to resistor networks to reduce EMI and RF noise susceptibility, are also shown in Figure 5.

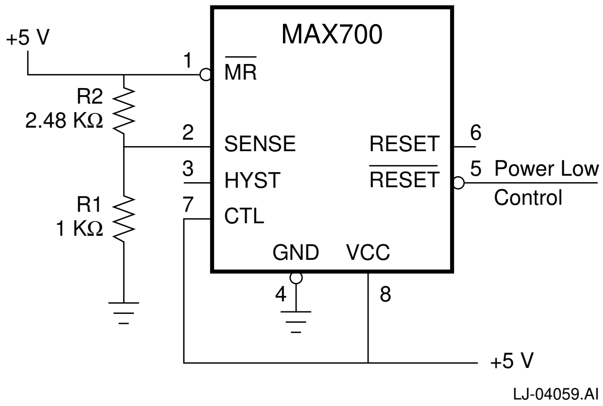
Figure 5 Magnetics Interface to the RJ45 Connector



3.1.4 Low Power Protection

During power changes, power-up and power down, an unpredicted sequence of bits may be transmitted to the network. This can cause line errors, collisions or even false packets on the network. To avoid unwanted sequences from being transmitted to the network, a dedicated subcircuit was implemented for low power protection. This subcircuit is shown in Figure 6.

Figure 6 Subcircuit for Low Power Protection



The subcircuit uses Maxim part number MAX700, which is configured to assert $\overline{RESET}$ (low) when its VCC supply voltage crosses a predefined low boundary—Vcross. Vcross is predefined by the values ratio of the two resistors that comprise of the voltage divider, according to the following formula:

$$Vcross = 1.29 * R2/R1 + 1$$

We have set Vcross to be

$$Vcross = 1.29 * 2.\quad 48/1 + 1 = 4.5V$$

Different values may be chosen for other implementations. $\overline{RESET}$ drives both the $\overline{FO}$ (Fiber-Optic Off) input to the MC68836 and the $\overline{TXOFF}$ input to the ML6671 transceiver. When $\overline{FO}$ is asserted into the MC68836, the MC68836 output pair, TDH and TDL, go into quiet state. When the $\overline{TXOFF}$ input to the ML6671 is pulled low, the MLT-3 transmitter is forced to the quiet state protecting the network from any unwanted interference.

Another way to prevent unwanted noise on the network during power-up uses the $\overline{LBK}$ input to the ML6671. A pulldown on this signal line is recommended so that on power-up the ML6671 will be in loopback mode disabling transmitting data. The ML6671 is changed to normal operating mode after the system is stable and the 21140 is initialized. This method requires driver software support.

Note

For specific designs, a fixed voltage controller can be used as well (MAXIM 80x).

3.2 10BASE-T Network Implementation

The 21140 10BASE-T network uses the standard, 7-wire connection to an external ENDEC Level One part number LXT901.

3.2.1 LXT901 ENDEC and Transceiver

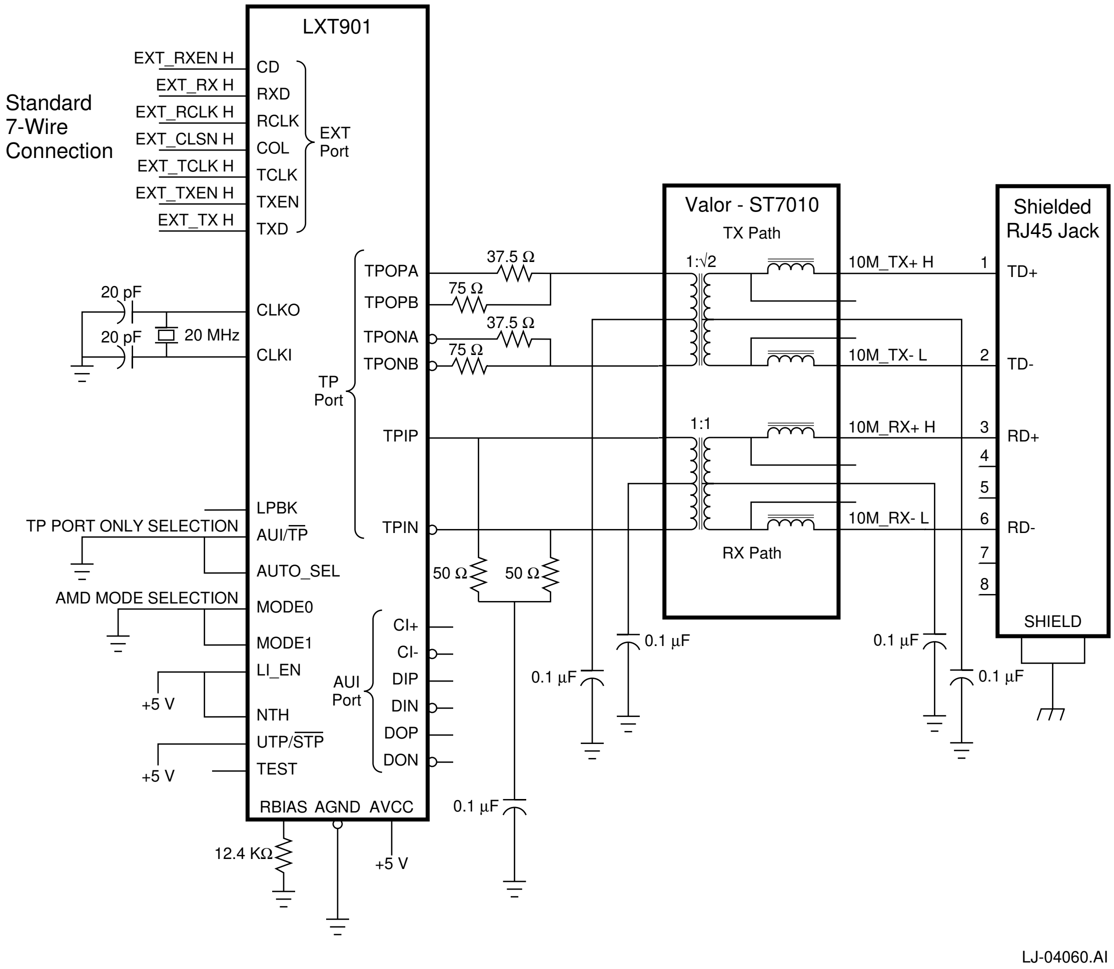
The LXT901 integrates all the required functions, including the network filters, and requires a minimum of external components and magnetics as shown in Figure 7.

The 21140 is fully compatible with the LXT901 AMD operation mode. This is the only mode that should be used for normal operation with the 21140.

The LXT901 requires a standard 100 PPM, 20-MHz crystal to operate the transmit and receive clocks. The LXT901 supplies the 21140 transmit clock.

The LXT901 support two loopback modes—internal loopback and external loopback (Sections 3.2.1.1 and 3.2.1.2).

Figure 7 LXT901 with External Components and Magnetics



3.2.1.1 Internal Loopback Internal loopback is controlled by the LPBK pin. Asserting the LPBK pin (high) allows the signal coming from the standard, 7-wire interface to pass through all the LXT901 transmit paths and to be looped back at the last LXT901 transmitter level through the LXT901 receive path and back out to the receive part of the standard, 7-wire connection.

While in the internal loopback mode of operation, the LXT901 also recovers the receive clock from the signals that are looped back. When the LXT901 is in this mode, no data is transmitted on the network transmit lines. The network RX lines will be ignored by the LXT901 while in this mode of operation.

The 21140 provides a very simple and convenient way to support loopback testing through one of its general-purpose pins (**gep<7:0>**).

3.2.1.2 External Loopback When in the external loopback mode of operation, the LXT901 disables all collision operation. This enables the signal coming from the standard, 7-wire interface to be transmitted to the network then looped back (by an external loopback connector) and come back through the LXT901 receive path.

The 21140 provides a very simple and convenient way to support loopback testing through one of its general-purpose pins (**gep<7:0>**).

4 Application-Specific Control and Monitor Functions

The 21140 provides eight general-purpose pins (**gep<7:0>**). Each of these pins can be configured to be either an input or an output pin. Their values can be read or written, respectively, by the driver software. These pins can be used for a variety of functions. Using such pins for various modes of loopback operation is discussed in Section 3. Other onboard control functions, such as LED indications and software hooks for hardware indication, can be implemented.

Refer to the *DECchip 21140 PCI Fast Ethernet Evaluation Board User Guide* for recommended implementations supported by software drivers supplied in the DECchip 21140 PCI Fast Ethernet Evaluation Board Kit.

The recommended implementation of **gep<7:0>** should be used. An implementation that is compatible to the support provided by the software drivers is acceptable. Incompatible implementations of **gep<7:0>** require modifications to the software drivers.

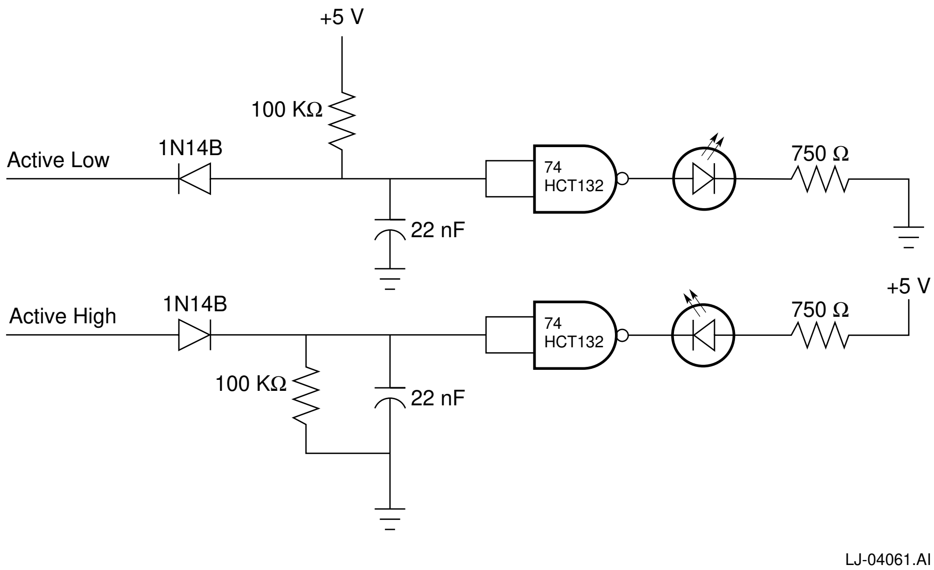
5 LED Support

The 21140 supports LED connection for receive, receive match, transmit, symbol link, and port select indication.

5.1 Receive/Transmit LED Support

The receive/transmit indication can be implemented by LEDs such as those shown in Figure 8. The pulse stretching logic for active low and active high signals is also included in Figure 8.

Figure 8 Time Stretching Logic



Note

The value of the 750-ohm resistor shown in Figure 8 depends on the rating of the LED used and the required lighting level.

The pulse width stretcher circuit connected to each LED stretches the period that the light is on so that it is noticeable to the human eye (20 ms).

- The receive activity LED is activated by the 21140 pin **rcv_match_h** (pin 122). This pin is asserted when a received packet has passed the address filtering and is recognized by the 21140 as a packet directed to this station.
- The transmit activity LED is activated by 21140 pin **mii/sym_txen_h** (pin 125) for the 100BASE-TX connection. This pin is asserted when the 21140 is transmitting on the network and is activated for the 10BASE-T connection from the transmit LED pin (pin 19) on the LXT901.

5.2 Port Select and Link Indication LEDs

A dual-color LED is used here to indicate port select and link status. The LED color is green to indicate an established link and is red to indicate that no link is established. The LED can also be turned completely off indicating that the port is not selected by the 21140.

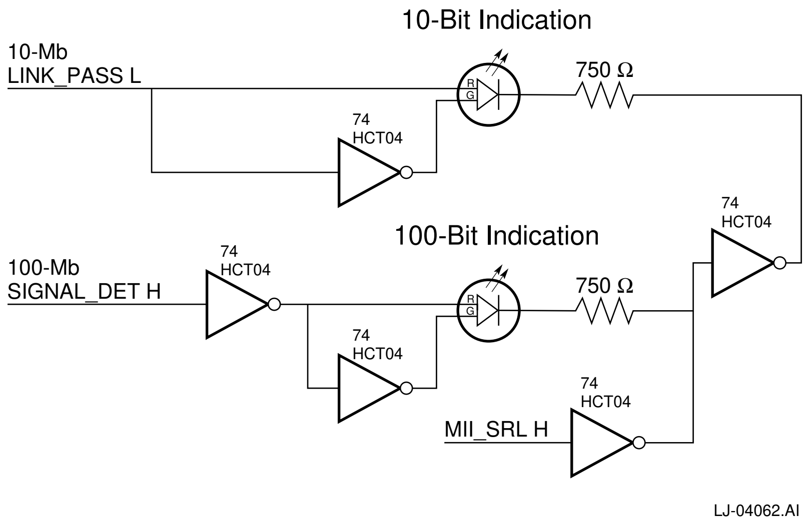
The circuit shown in Figure 9 is for an application that supports dual networks—100-Mb/s and 10-Mb/s. The **mii_srl** pin (pin 133) of the 21140 is used as the primary control signal that indicates which port is selected by lighting the LED for the port. Only one of the two LEDs can be on at a time.

The 100-Mb/s indication LED is controlled by the signal **SIGNAL_DET H** that is the signal detect indication from the 100BASE-TX symbol transceiver and clock generator and MII/SYM port interface chip (MC68836).

The 100-Mb/s indication LED can also be turned on by the **sym_link** pin (pin 124) of the 21140 allowing a link indication only when the 21140 is synchronized to the incoming symbol stream and when a valid symbol flow is identified by the 21140.

The 10-Mb/s indication LED is driven by the signal **LINK_PASS L** from the 10-Mb/s ENDEC (LXT901) based on the appearance of link pulses or valid data on the receive line.

Figure 9 100-Mb/s and 10-Mb/s Link and Port Select Indication



6 3.3-Volt Power Supply

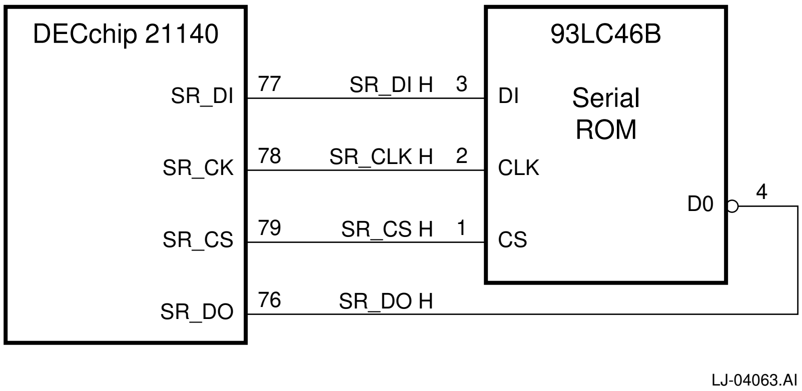
The 21140 operates from a 3.3-V power supply. The Linear Technology LT1117 regulator is recommended for the dc conversion. A 10-µF capacitor should be connected across the 5-V input, and a 47-µF capacitor should be connected across the 3.3-V output to stabilize those voltages.

Decoupling capacitors on the 21140 supply pins are recommended. Capacitors with the values of 0.1 µF, 0.01 µF, and 10 µF are suggested.

7 Serial ROM Port

The 21140 provides a standard MicroWire port to interface any MicroWire serial ROM. The serial ROM should contain the unique Ethernet address and any additional board-specific information. Each Ethernet adapter must have a unique Ethernet address for the adapter. National 93LC46B, MicroWire, or a compatible serial ROM is recommended. The serial ROM signals are shown in Figure 10 and should be connected directly to the matching pins of the 21140.

Figure 10 Serial ROM Connections



Note

Software support is required to program and read the serial ROM.

8 PCB Layout Recommendations

This section presents PCB layout recommendations for the design of 100BASE-TX and the 10BASE-T connections, and it describes how to combine them on a single PCB. Because of the mixture of high-speed digital signals and very high-speed analog/ECL signals, these recommendations should be implemented.

8.1 PCI Signals Routing

The 21140 is designed to support the PCI local bus standard where the pins are arranged in the same order as the PCB edge connector so that signal lines may be kept to PCI standard length limits. The length limit is 1.5 inches for etch lines and 2.5 inches for PCI clock lines.

8.2 100-Mb/s PCB Layout Considerations

The following items should be considered when performing PCB layout for 100-Mb/s circuits.

8.2.1 21140 to MC68836 Connection

The data lines should be kept as short as possible and should not have significant differences of length and characteristics between lines within groups such as **mii/sym_rxd<4:0>** and **mii/sym_txd<4:0>**.

Distribution of the 25-MHz transmit clock should be carefully handled to avoid skew and clock noise. When there are long lines (over 3 inches) a clock driver should be considered. Clock lines should be routed in the external layers of the PCB.

The recovered RX clock routing should be handled carefully in an external routing layer, and termination should be added for long lines (over 3 inches).

8.2.2 MC68836 External Components

External components connected to the MC68836 transmit clock lines, PLL signal lines, and RX clock lines should be placed as close as possible to the MC68836. Their signal lines should be routed as directly as possible to the MC68836 pins.

The RX clock recovery crystal (20.833333 MHz) might require tuning of the capacitors based on the layout design of the PCB.

8.2.3 MC68836 to ML6671 Connection

The signal line pairs connecting the MC68836 and the ML6671 parts are very high-speed (125 MHz), sensitive lines. These lines should be kept as short as possible and should be routed on external routing layers. The lines should be routed as pairs, avoiding as much as possible differences between the two lines of each pair.

The signal lines should be terminated as noted in Section 3.1.1.2. The termination nets should be kept as close as possible to the chip pad and should be placed on the receiving side of the lines. First, connect the two pads of the chips; only then add the termination connection to the chip pad and *not* to the chips' connecting etch line. Keep the pairs as far apart as possible to avoid unnecessary crosstalk.

8.2.4 ML6671 to Network Connection

Keep all signal lines as short as possible, especially the RX lines, which are the most noise-sensitive lines. Separate the RX lines from the TX lines to avoid crosstalk. Route all line pairs together and with as little difference as possible between the two lines in each pair. If the system is noisy, improve noise immunity by routing the receive and transmit pairs with surrounding ground etch. Place all the ML6671 external components as close as possible to the connecting pads.

8.3 10-Mb/s PCB Layout Considerations

The following items should be considered when performing PCB layout for 10-Mb/s circuits.

8.3.1 21140 to LXT901 Connection

Keep the signal lines as short as possible and route the RX and TX clocks first, with traces as short as possible. Separate the RX lines and the TX lines to avoid crosstalk.

8.3.2 LXT901 External Components and Network Connection

Place the external components as close as possible to the LXT901. Place the crystal capacitors as close as possible to the LXT901, with traces as short as possible. Connect the network lines in pairs and separate the transmit pair from the receive pair. Pay special attention to the network RX lines, which are the most noise-sensitive of this connections group.

8.4 Ground and Power Planes

Implementing a design with the 21140 requires handling three kinds of power signals:

- VCC (5 V) power for all network ENDEC and 21140 external components
- VDD (3.3 V) power for the 21140 chip
- GND (common ground)

Use two power planes on the PCB—VCC and GND.

VDD power can be supplied by either a cut in the VCC power plane or by a power island under the 21140 chip on one of the signal routing layers.

Add decoupling capacitors to all power supplies. Place the decoupling capacitors as close as possible to the power pads of the chips.

Cut the VCC and GND planes between the 100-Mb/s signaling area and the 10-Mb/s signaling area to avoid any interference between the two ports.

For specific power recommendation of the MC68836 and ML6671, refer to the documentation for each chip.

9 Other Considerations

If the JTAG port is unused, then **tck** (pin 141), **tdi** (pin 143), and **tms** (pin 142) should be pulled up to VDD (3.3 V), while **tdo** (pin 144) should remain unconnected.

Technical Support and Ordering Information

Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

Ordering Digital Semiconductor Products

To order the DECchip 21140 PCI Fast Ethernet LAN Controller and evaluation board, contact your local distributor.

You can order the following semiconductor products from Digital:

Product	Order Number
DECchip 21140 PCI Fast Ethernet LAN Controller	21140–AA
DECchip 21140 Evaluation Board Kit	21A40–03

Ordering Associated Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line. For ordering information, see the Ordering by Telephone and Through Direct Mail section.

Title	Order Number
DECchip 21140 PCI Fast Ethernet LAN Controller Product Brief	EC–QC0AA–TE
DECchip 21140 PCI Fast Ethernet LAN Controller Data Sheet	EC–QC0BA–TE
DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual	EC–QC0CA–TE
DECchip 21140 PCI Fast Ethernet Evaluation Board User's Guide	EC–QD2SA–TE

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